REMARKS

The drawings stand objected to for improper cross hatching and for failure to label figures 13-15 as "prior art". The drawings have been amended herein above to correct the cross hatch and to provide the "prior art" labeling remarked upon by the Examiner. A marked up copy of the drawing amendments is attached. A new/ substitute copy of the formal drawings is also attached.

The specification stands objected to for typographical errors on pages 1 and 3 remarked upon by the Examiner. These pages of the specification have been amended to overcome this objection, consistent with the Examiner's remarks. A marked up copy and a clean copy of these amended pages is attached.

Claim 9 stands rejected under 35 USC 112 for the term "spacing distance". This claim has been amended to recite the terminology of the specification, namely - - distance between the terminals - -.

Independent claim 1 and independent claim 40 have been amended to add the additional limitation of: - - the connecting terminal being provided on its surface with solder material - -.

New dependent claim 53 has been added to depend from amended claim 1 and new dependent claim 54 has been added to depend from amended claim 40. Each of these new dependent claims adds the limitation: - - wherein the wiring lines of the respective wiring line layers below the connecting terminals are arranged at the same density as the density of connecting terminals so as to be each located under a respective connecting terminal - -.

Claims 1-4, 7-24, and 40-46 have been examined. Of these claims 1-4, 7-8, 40-41 stand rejected under 35 USC 102(e) as anticipated by Echigo et al. (6,274,821). Claims 10-24 and 42-46 stand rejected under 35 USC 103(a) as obvious in view of Echigo (6,274,821). Claims 16, 17 stand rejected under 35 USC 103(a) as obvious in view of Echigo (6,274,821) combined

with Hsu (6,242,815). Claims 19-24 stand rejected under 35 USC 103(a) as obvious in view of Echigo (6,274,821) combined with Takubo (6,329,610) and Noda (5,841,190) and Yoshikawa (5,796,165). The Examiner has remarked that Echigo does not disclose the width and spacing of terminals wiring and via.

Echigo is relied upon to show a surface-mounting substrate for mounting a part thereon, which has a core, a plurality of layers of patterned wiring lines separated from each other by an insulation layer interposed there between and bias piercing through the insulation layer to connect wiring lines at adjacent layers. Regarding claim 2-3, the Examiner has remarked that Echigo discloses electrode 10 soldered to the terminal.

The Examiner has admitted that Echigo does not address the uniform density of terminals nor the internal wiring pattern claimed by the applicant. The Examiner, however, in supporting his rejection has presumed that the terminals on the top surface will depend upon the number of electrodes on the semiconductor device to be connected and the arrangement and wiring pattern will be arranged to get the maximum possible component density of the component mounting pad without compromising the quality of the board, such as withstanding thermal expansion, contraction without warping or cracking, a better heat dissipation rate, rigidity and avoiding short circuiting.

Once he has read applicant's specification, the Examiner concludes that it is a matter of common sense to have uniform distribution of the features to have the above advantages. He further concludes that it would be obvious to provide a uniformly distributed terminal arrangement to get higher component density without compromising quality and to improve reliability. THIS CONCLUSION AND ANALYSIS IS TRAVERSED.

The Examiner has also expressly admitted that Echigo does not address a power or ground layer claimed by applicant in claims 14 and 18. He has remarked that both power layers

and ground layers were known and it would be obvious to provide Echigo with same. THIS CONCLUSION AND REASONING IS TRAVERSED.

In rejecting claims 16, 17, the Examiner has admitted that Echigo does not address a dummy member. Again the Examiner remarks that dummy layers are known in the art for maintaining the uniformity of a member, increasing strength or rigidity, or allowing for future changes. The Examiner states that Hsu discloses dummy pads for increasing the rigidity and strength of the mount area.

In rejecting claims 19-24 the examiner admits that Echigo does not address the width and spacing of terminals, spacing of wiring, or spacing of via. The Examiner concludes that these features will depend upon the type of material used, current carrying capacity, manufacturing process and space available. THIS LOGIC IS TRAVERSED.

The Examiner reasons that since Noda and Takubo disclose a via with a 50 micrometer diameter and Yoshikawa discloses wiring with a 200 micrometer width, it would be obvious to modify Echigo to these dimensions, in order to meet the component density, signal transmission capacity and resultant reliable circuit board. THESE CONCLUSIONS ARE TRAVERSED.

The present invention has terminals, which are filled in an outermost insulation layer provided at the surface of the surface-mounting substrate, in such a manner that the entire surface of the connecting terminal is exposed at the surface of the surface mounting substrate. The present invention has the surface of the connecting terminal at substantially the same level as the level of the surface of the outermost insulation layer, and the connecting terminal is provided on its surface with solder material.

The present invention also has a wiring layer or layers below the wiring line layer having the connecting terminals formed so as to have a uniform wiring line density, and for this purpose may utilize dummy members, i.e., wiring layers which are not electrically connected. These dummy members are not insulation layer, but dummy conductive layers This permits a uniform

manufacturing process regardless of chip mounted and regardless of which wiring layers are electrically connected and which are dummy..

In the present invention, since the entire surface of the connecting terminal is exposed at the outer surface of the surface-mounting substrate, the surface of the connecting terminal is at substantially the same level as the surface of the outermost insulation layer of the surface-mounting substrate. The surface area of the connecting terminal can be adequate and the run-out of melted solder from the area of the connecting terminal can be avoided, even if the connecting terminal has a reduced size.

With the present invention, if the pitch (spacing distance) of adjacent connecting terminals became small, a short-circuit between adjacent terminals caused by solder can be avoided. The present invention thereby permits a high density for connecting terminals. The surface-mounting substrate can be made with an increased number of terminals and a decreased size. Moreover, the design of the present invention permits this high density without decreasing surface area, therefore, a mounting part, such as a semiconductor chip, which has an large number of terminals can be mounted on the substrate without lowering mounting strength.

With the present invention the wiring line layer and the layers below the wiring line layer have connecting terminals formed with a uniform wiring line density, with or without dummy (wiring line layer) members. The dents at the connecting terminal can be uniform. All of the terminals of the mounting part (the chip) can be securely bonded to the surface-mounting substrate.

Echigo shows a wiring pattern 11 (connecting terminal) having the periphery covered by a soldering resist layer 13. Echigo is limited to a conventional structure which cannot pervent melted solder from running out. Echigo does not show nor suggest that the entire surface of the connecting terminals being exposed at the outer surface of the surface-mounting substrate.

Echigo does not show nor suggest that the surface of the connecting terminals be at substantially the same level as the level of the surface of the outer most insulation layer of the surface mounting substrate.

Echigo does not show nor suggest providing solder on the wiring pattern in advance. Echigo does not consider the problems, which the present invention solves. In Echigo, members 10, 12 are solder balls provided on flip-chip 8. This is not what is disclosed and claimed in the present invention. Moreover, Echigo covers the periphery of his wiring pattern 11 with a solder resist layer 13, thereby greatly reducing the exposed portion of the wiring pattern 11 and the mounting strength of a mounting part.

These features of the present invention are recited in amended claims 1 and 40. Therefore, these claims as amended differentiate over the cited art and are now allowable. The dependent claims should likewise be allowed.

Hsu shows a flexible film mono-layer substrate 220 with what he characterizes as a dummy pad 220f. However, Hsu's dummy pad 220f is merely a series of areas of material deposited on top surface of his mono-layer substrate film 220 in a pattern, i.e, a square, circle, star, etc. (see 200f on figs. 7, 8, 9 of Hsu). The Hsu pad 220f does not anticipate nor obviate applicant's structure.

Yoshikawa is limited to an integrated circuit, itself, and does not address a substrate. Yoshikawa is non-analogous art and cannot be combined with Echigo. Noda shows a printed wiring board 12 with a mono-layered insulating substrate 16 with a built up section 17. However, Noda's structure neither shows nor suggests the structure now claimed by applicant.

Claims 1,40, 41 as now amended differentiate the present invention over the cited prior art, read separately and in combination.

Respectfully submitted,
Paul & Paul

Date: 7/26/02

by: John J. Simkanich
Regis. No. 26,036
2000 Market Street
Philadelphia, PA 19103
(215) 568-4900
FAX 215-567-5057

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Commissioner for Patents
Washington, D.C. 20231

on 7/26/02
(date)

PAUL & PAUL
by: John J. Simkanich

(signature)